UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,157	03/09/2006	Toshiaki Takenaka	2006-0223A	3496

52349 7590 08/04/2008

WENDEROTH, LIND & PONACK L.L.P.
2033 K. STREET, NW
SUITE 800
WASHINGTON, DC 20006

EXAMINER	
GOFF II, JOHN L	

ART UNIT	PAPER NUMBER
1791	

MAIL DATE	DELIVERY MODE
08/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,157	TAKENAKA ET AL.	
	Examiner	Art Unit	
	John L. Goff	1791	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/9/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 5-8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 requires "applying heat and pressure to the laminated structure". This step is unclear as the structure is not laminated until the heat and pressure is applied. The limitation is interpreted as applying heat and pressure to form the laminated structure.

5. Claim 12 requires "A method of manufacturing a multi-layer circuit board". The preamble is unclear as the body of the claim does not specifically require any steps that

manufacture the multi-layer circuit board. The preamble is interpreted as in a method of manufacturing a multi-layer circuit board an improvement comprising.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1, 3, 5-9, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Specification pages 1-4, 8, and 9) in view of Pommer (U.S. Patent 6,560,844).

The admitted prior art discloses a conventional method of manufacturing a multi-layer circuit board comprising providing a structure including a core circuit board having a circuit pattern thereon and a prepreg sheet having a through-hole filled with conductive paste sandwiched between a pair of metal foils further sandwiched between a pair of lamination plates

and applying heat and pressure to form a laminated structure (Figures 6A-6D and Page 3, line 6 to Page 4, line 8). The admitted prior art does not specifically teach the lamination plates are selected to have a thermal expansion coefficient (TCE) equivalent to a TCE of the core circuit board. However, selecting lamination plates to have a TCE equivalent to a layer of the laminated structure was known as evidenced by the admitted prior art wherein a TCE equivalent to the metal foil is chosen to prevent wrinkling. Further, it was known in the art that each layer of the laminated structure, e.g. a structure including circuit board and prepreg layers as depicted in Figure 1, should have substantially similar considered equivalent TCE and that the lamination plates are selected to have a TCE the same as the TCE of the layers as shown by Pommer to prevent distortion of the layers (Figures 1 and 3 and Column 2, lines 3-5 and 44-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to practice the method as taught by the admitted prior art wherein all of the layers of the structure have equivalent TCE to prevent distortion of the layers as taught by Pommer thereby including selecting a lamination plate whose TCE is equivalent to the core circuit board.

Regarding claim 3 and 6, the admitted prior art teaches the core circuit board has four or more layers. The admitted prior art teaches the core circuit board and the prepreg sheet are alternately laminated so as to have two or more layers.

Regarding claims 7 and 8, the admitted prior art further teaches a buffer material considered formed of a material capable of accommodating difference in TCE between the lamination plate and a carrying plate disposed outside the structure which structure is placed on a heat press plate considered the carrying plate such that heat and pressure goes through the buffer material and the carrying plate. It would have been obvious to one of ordinary skill in the art at

the time the invention was made to practice the method as taught by the admitted prior art wherein all of the layers in the lamination have equivalent TCE to prevent distortion of the layers as taught by Pommer thereby including selecting a carrying plate whose TCE is equivalent to the lamination plate.

Regarding claim 9, the admitted prior art teaches the prepreg sheet contains a base and a resin layer impregnated with the base to form a resin layer on both surfaces of the base.

Regarding claims 11 and 12, Pommer is considered to require measuring the TCE of all of the layers including the core circuit board otherwise selecting a lamination plate with an equivalent TCE would not be possible.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 5-9, 11, and 12 above, and further in view of Ikeguchi et al. (JP 57011026 and see also the abstract).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 2 except for a specific teaching that the thickness of the resin layer formed on both sides of the base is at least 20 microns in total thickness. Ikeguchi disclose a prepreg excellent in workability comprising a base and a resin layer impregnated with the base to form a resin layer on both sides of the base having at least 20 microns in total thickness (See the abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the resin layers on both sides of the base as taught by the admitted prior art as modified by Pommer with a thickness at least 20 microns in total as shown by Ikeguchi to form a prepreg excellent in workability.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 5-9, 11, and 12 above, and further in view of Shirasawa et al. (U.S. Patent 4,614,559).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 4 except for a specific teaching that the core circuit board is not less than one time as thick as the prepreg sheet. Shirasawa directed to manufacturing a multi-layer circuit board comprising core circuit boards and prepreg sheets teach the layers are desirably as thin as possible to form a dimensionally stable board including specifically demonstrating the core circuit boards are not less than one time as thick as the prepreg sheets (Column 1, lines 33-35 and Tables 1 and 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the core circuit board and prepreg sheet in the admitted prior art as modified by Pommer layers as thin as possible including wherein the core circuit board is not less than one time as thick as the prepreg sheet as shown by Shirasawa to form a multi-layer circuit board that is thin and dimensionally stable.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 5-9, 11, and 12 above, and further in view of Del (U.S. Patent 4,180,608).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 10 except for a specific teaching that the base is woven and the resin is B-staged. It is considered extremely well known in the art that a prepreg generally comprises a woven base and a B-staged resin as evidenced by Del (Column 4, lines 23-27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the prepreg taught by the

admitted prior art as modified by Pommer as was generally well known including a woven base and a B-staged resin as evidenced by Del only the expected results being achieved.

12. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 5-9, 11, and 12 above, and further in view of Levit (U.S. Patent Application Publication 2005/0230072).

The admitted prior art and Pommer as applied above teach all of the limitations in claims 11-14 except for a specific teaching that the TCE for each layer is measured by measuring the TCE at two positions or more in a range from room temperature to a heat pressing temperature by using a thermomechanical measurement apparatus and calculating an average value of the TCE from the two positions or more, it being noted Pommer is not limited to any particular technique for measuring the TCE for each layer. Levit is exemplary of measuring the TCE of a layer for use in a circuit board wherein determining the TCE for the layer includes measuring the TCE at two positions or more in range from room temperature to a heat pressing temperature by using a thermomechanical measurement apparatus and calculating an average value of the TCE from the two positions or more (Paragraphs 0011, 0030, and 0038). It would have been obvious to one of ordinary skill in the art at the time the invention was made to measure the TCE for each layer of the structure taught by the admitted prior art as modified by Pommer to determine that each layer has an equivalent TCE as required by Pommer wherein a known suitable technique for determining the TCE was disclosed by Levit.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571) 272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John L. Goff/
Primary Examiner, Art Unit 1791